

## REMARKS/ARGUMENTS

### Claim rejections 35 U.S.C. § 112

The rejection asserts that because the Applicant's response specifically pointed to page 27, line 5 through page 28, line 8 and because Claims 6 and 14 were also supported by the same disclosure in accordance with 35 U.S.C. §112, first paragraph, the limitation of Claim 1 wherein "the virtual microcontroller having means for detecting an I/O read instruction followed by a conditional jump instruction" is interpreted as equivalent to the structure, material, or acts encompassed by the claim language of Claims 6 and 14 reciting "detecting an I/O read instruction followed immediately by a conditional jump instruction." The Applicant respectfully submits that the Examiner's interpretation is unduly narrow because the mere fact that two claims are supported by the same portion of the specification does not necessarily translate to them being equivalent. Moreover, Claim 1 specifically invokes 35 U.S.C. §112, sixth paragraph and should be interpreted in light of the entire specification and equivalent thereof and not in light of other claims as suggested by the rejection.

It is respectfully asserted that Claim 1 complies with 35 U.S.C. §112, first and sixth paragraph. The example to follow is to illustrate that there is support in the specification and not intended to limit the scope of Claim 1.

The Examiner is respectfully directed to page 27 line 5 to page 28 line 8 of the specification, reciting that virtual microcontroller computes the target jump location as the I/O data is being received and that before the actual jump the virtual microcontroller evaluates the conditional jump and either uses the pre-computed jump information if the condition is true or that it simply increments the program counter otherwise. It is understood by those skilled in the art that such detection can be purely hardware based (e.g., combinational logic), software based (e.g., sequential logic), or some combination of the two. As such, independent Claim 1 is fully supported by the specification and complies with the written description requirement, under 35 U.S.C. §112, first paragraph.

Moreover, the Examiner is respectfully directed to page 27 lines 14-16 of the specification, reciting that an instruction is received and a determination is made whether or not an I/O read followed by a conditional branch operation. Accordingly, the Examiner's interpretation for limiting the scope of Claim 1 to that of Claims 6 and 14, an I/O read followed immediately by a conditional branch operation, merely because they are supported by the same portion of the specification is unduly narrow and inappropriate. As such, Claim 1 complies with the requirements of 35 U.S.C. §112, first and sixth paragraph and should be interpreted to recite a limitation whereby I/O read is followed by a conditional jump operation, as claimed.

Claim rejections 35 U.S.C. § 103

Claims 1-4, 6-11 and 13-19 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over U.S. Pat. No. 6,366,878 (hereinafter, Grunert) in view of "Structured Computer Organization, Fourth Edition" by Andres S. Tanenbaum with contribution by James R. Goodman (hereinafter, Tanenbaum). The Applicant respectfully traverses.

Independent Claim 1 recites a limitation whereby a virtual microcontroller and a microcontroller execute instructions in lock-step by executing the same instructions using the same clocking signals, as claimed. Moreover, independent Claim 1 recites a limitation whereby the microcontroller sends I/O read data to the virtual microcontroller, as claimed.

Grunert discloses that the master microcontroller feeds the memory address to the external memory component (see Grunert, col. 4, lines 41-44). Data byte from the external memory component is then read out and fed to the master microcontroller and the slave microcontroller (see Grunert, col. 4, lines 47-53). The master processes the operating program and feeding the operating program to the slave serves the purpose of properly timing the control of data input and output to external connections of the overall circuit arrangement (see Grunert, col. 4 line 67 to col. 5 line 5). Accordingly, the master microcontroller sends the memory address and as a result data byte read out is fed to both the

master and the slave microcontrollers. As such, Grunert fails to disclose or suggest that the microcontroller sends I/O read data to the virtual microcontroller, as claimed but instead discloses that the external memory component sends data byte read out to both the master and the slave microcontrollers.

Moreover, Grunert discloses that the data D read out from the memory are also fed to the slave (see Grunert, col. 4, lines 29-53) and that a clock system ensures good synchronization between master and slave (see Grunert, col. 5, lines 8-9). The rejection inappropriately presumes that based on this disclosure, execution of the same instruction using the same clocking signal, as claimed follows. The Applicant respectfully disagrees because the mere fact that the data D read out is fed to both master and slave and that good synchronization between master and slave exists does not necessarily translate to execution of the same instructions using the same clocking signals, as claimed. For example, the data D read out may be fed to both master and slave with good synchronization between the two microcontrollers, however, processing of data D read out by the slave may be significantly after processing of data D read out by the master. Grunert fails to explicitly disclose or suggest virtual microcontroller and the microcontroller executing the same instruction using the same clocking signal, as claimed.

In fact, Grunert teaches away from execution of the same instruction using the same clocking signals, as claimed. Grunert discloses that the slave microcontroller ports P0', P2' and P3' serve as external connections of the overall circuit arrangement (see Grunert, col. 4, lines 59-61) and that feeding the operating program to the slave microcontroller serves the purpose of properly timing the control of the data input and output via the ports P0', P2' and p3' (see Grunert, col. 5, lines 3-5). Therefore, feeding the operating program to the slave microcontroller provides proper timing with external connections of the overall circuit arrangement and not with the master microcontroller (see Grunert, Figure 1). As such, Grunert teaches away because the purpose of feeding the operating program to the slave microcontroller is not execution of the same instructions using the same clocking signals by the virtual microcontroller and the microcontroller, as claimed but is instead to provide proper timing between the slave microcontroller and external connections of the overall circuit arrangement.

The rejection admits that Grunert fails to disclose the limitations regarding "means for detecting an I/O read instruction followed by a conditional jump instruction, and for computing a conditional jump address prior to receipt of I/O read data from the microcontroller to remain in lockstep execution with the microcontroller," as claimed. Moreover, the rejection admits that Grunert fails to disclose the limitation regarding "means for determining after receipt of the I/O read data from the microcontroller whether to proceed with instruction execution

at a next consecutive address at the conditional jump address,” as claimed. The rejection relies on Tanenbaum to show these limitations. The Applicant respectfully traverses.

Tanenbaum discloses that what most machines do when they hit a conditional branch is to predict whether it is going to be taken or not and if a branch is correctly predicted execution continues at the target address (see Tanenbaum, page 272). Accordingly, Tanenbaum discloses predicting whether to take a conditional branch when a conditional branch is hit and not computing a conditional jump address prior to receipt of I/O read data from the microcontroller, as claimed.

Moreover, the rejection does not address the limitation whereby the virtual microcontroller having means for detecting an I/O read instruction followed by a conditional jump instruction to remain in lockstep execution with the microcontroller, as claimed. Moreover, the Applicant does not understand Tanenbaum to disclose or suggest the recited limitation.

Accordingly, the Grunert alone or in combination with Tanenbaum fails to render independent Claim 1 obvious, under 35 U.S.C. §103(a). Independent Claims 6 and 14 are similar in scope to that of independent Claim 1 and are patentable for similar reasons. Dependent claims are patentable by virtue of their

dependency. As such, allowance of Claims 1-4, 6-11 and 13-19 is earnestly solicited.

Claims 5, 12 and 20 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Grunert in view of Tanenbaum and further in view of U.S. Pat. No. 6,173,419 (hereinafter Barnett). The Applicant respectfully traverses.

The rejection admits that the combination of Grunert and Tanenbaum fails to teach that virtual microcontroller is implemented in a field programmable gate array (FPGA), as claimed. The rejection relies on Barnett to remedy this failure. The Applicant, however, does not understand Barnett to remedy the failures of Grunert and Tanenbaum as discussed above with respect to independent Claim 1. Accordingly, the addition of Barnett to the combination of Grunert and Tanenbaum does not teach the limitations of independent Claim 1. Accordingly, the addition Barnett to the cited combination does not render Claims 5, 12 and 20 obvious, under 35 U.S.C. §103(a). As such, allowance of Claims 5, 12 and 20 is earnestly solicited.

For the above reasons, the Applicant requests reconsideration and withdrawal of these rejections under 35 U.S.C. §112 and 35 U.S.C. §103.

### CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-20 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-20 overcome the rejections of record and, therefore, allowance of Claims 1-20 is earnestly solicited.

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